SubCkt.vhd

```
--============================================================--
--
-- A PECL Rate-Generator Sub-Circuit modeling for MTI/Vsys
--
--  SubCktRateGen.vhd  ( DEMO vsn )
--  -----------------   ----------
--
-- compile followings in advance
--  BasePack.vhd
--  EL58.vhd
--  EL31.vhd
--  E016Pack.vhd
--  E016.vhd
--  PECL_Comp.vhd

-- ========================================================== --
--  Block descriptions   ( In detail, refer to VHD source)
-- ---------------------------------------------------------- --
--
--  Mode ------+           ProgValue
--             |             |
--           +-*--+     +----*----+
-- pLOAD --->|a   |     |         |           nTC
--           |    |     |      nTC|O-+---------------+
-- pSTEP --->|b   |O--->|nCE      |  |               |
--           +----+     |         |  |             +-*--+
--             |     +->|nPE      |  |      GND/-->|a   |-->TCSS
--           +-*--+  |  +---------+  |  +-----+    |    |
-- VCC /---->|a   |  |   EL16        +->|D   Q|--->|b   |
--           |    |  |                 |  |     |    +----+
--       +-->|b   |O-+                 |  |     |     EL58
--       |   +----+                    |  +-----+
--       |    EL58 Mpx                 |    EL31
--       +-----------------------------+
--
--              ( "nTC" net wiring will be a critical one. )
--

library ieee;
use ieee.Std_Logic_1164.all;
use ieee.Std_Logic_unsigned.all;
use work.BasePack.all;
use work.PECL_Comp.all;
  -- Using a component package permits eliminating "component
  -- declarations" in the following archtecture block.

--============================================================--
Entity SubCktRateGen  is
  generic( SbCktName : string := "SubCkt" ); -- Default name
  port( CLOCK       : in    Std_Logic;
        CLR         : in    Std_Logic;
        ModeLatch   : in    Std_Logic;
        ProgValue   : in    BYTE;
        pLOAD       : in    Std_Logic;
        pSTEP       : in    Std_Logic;
        nTCOUT      : out   Std_Logic;
        pTCSS       : out   Std_Logic;
        nTCSS       : out   Std_Logic    );
end SubCktRateGen;

```

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--============================================================--
Architecture Subckt of SubCktRateGen is
    signal nTC      : Std_Logic;    -- Terminal Count
    signal nPE      : Std_Logic;    -- Pararell load enable
    signal nCE      : Std_Logic;    -- Count enable
    signal NetVCC   : std_logic :='1';
    signal NetGND   : Std_Logic :='0';
    signal DFF_Q    : Std_Logic;
-------------------------------------------------------------
-- Here, I do not describe any component declarations.
-------------------------------------------------------------
Begin
    nTCOUT <= nTC;

COUNTER: E016   -- Counter Rategen  Wiring ---------------------
 generic map(InstName => SbCktName )
 port map(  CLK => CLOCK,        -- from 89429/etc
            MR  => CLR,          -- Initial reset.
            PIN => ProgValue,
            nPE => nPE,          -- Pararell load enable input
            TCLD=> ModeLatch,    -- If high,reload ProgVal at nTC

            nCE => nCE,          -- If low,counting op is enabled
            nTC => nTC,          -- Will be low at TerminalCount.
            Q   => OPEN );

MpxCE: EL58     -- This SY100EL58 used as a nCE gate.-----------
 port map(  SELIN=> ModeLatch,  -- When high,nCE will be locked,
            Da   => NetVCC,     -- low,else nCE becomes not(nTC)
            Db   => nTC,
            pQ   => OPEN,
            nQ   => nCE     );

MpxPE: EL58     -- This SY100EL58 used as a nPE gate. ----------
 port map(  SELIN=> ModeLatch,
            Da   => pLOAD,      -- Initialize pulse input
            Db   => pSTEP,      -- External Step input (clock'd)
            pQ   => OPEN ,
            nQ   => nPE     );

DFFnTC: EL31   -- This DFF is to provide a single clock pulse -
 port map(  S   => NetGND,
            R   => CLR,
            D   => nTC,
            CLK => CLOCK,
            pQ  => DFF_Q,
            nQ  => OPEN  );

GATEnTC: EL58   -- Functions in conjunction with DFFnTC:EL31. --
 port map(  SELIN=> nTC,
            Da  => NetGND,
            Db  => DFF_Q,
            pQ  => pTCSS ,
            nQ  => nTCSS    );

end Subckt;
```