PeclComp.vhd

```vhdl
--=========================================================--
--  A simple DEMO for ECL behaviour modeling.
--  -------------------------------------------------------
--      File name    :  PECL_Comp.vhd
--      Title        :  PECL counter
--      Library      :  WORK
--
--    by Yoshiaki Naruse    1998 9/9  Systems Workshop Inc.
--  -------------------------------------------------------

library ieee;
use ieee.Std_Logic_1164.all;
use ieee.Std_Logic_unsigned.all;
use work.BasePack.all;

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Package PECL_Comp is

constant PECL_PULLUP    : Std_Logic :='1';
constant PECL_OPEN      : Std_Logic :='0';

component E016  -- See E016.vhd (SIM-ONLY model)
    Generic( InstName   : string );
    PORT(   CLK,MR,TCLD,nPE,nCE     : IN Std_Logic;
            PIN                     : IN BYTE;
            nTC                     : OUT Std_Logic;
            Q                       : OUT BYTE  );
end component;

component E141  -- See E141.vhd  (SIM-ONLY model)
    PORT(   CLK,MR      : IN Std_Logic;
            SEL0,SEL1   : IN Std_Logic;
            DL,DR       : IN Std_Logic;
            Da,Db,Dc,Dd,De,Df,Dg,Dh : IN    Std_Logic;
            Qa,Qb,Qc,Qd,Qe,Qf,Qg,Qh : OUT   Std_Logic   );

end  component;

component EL58  -- See EL58.vhd  (SIM-ONLY model)
    PORT(   SELIN   : IN  Std_Logic;
            Da,Db   : IN  Std_Logic;
            pQ,nQ   : OUT Std_Logic );
end component;

component E163  -- See E163.vhd  (SIM-ONLY model)
    PORT(   SEL2,SEL1,SEL0  : IN  Std_Logic;
            AIN,BIN         : IN  Std_Logic_Vector(7 downto 0);
            pQA,nQA,pQB,nQB : OUT Std_Logic );

end component;

component E431  -- See E431.vhd (SIM-ONLY model)
    PORT(   pCK, nCK    : IN Std_Logic;
            pD,  nD     : IN Std_Logic;
            S,   R      : IN Std_Logic;
            pQ,  nQ     : OUT Std_Logic );
end component;

component EL31 -- See EL31.vhd (SIM-ONLY model)
    PORT(   S,R     : IN  Std_Logic;
            D,CLK   : IN  Std_Logic;
            pQ,nQ   : OUT Std_Logic );
end  component ;
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        component SubCktRateGen -- functional sub circuit model
          generic( SbCktName : string := "SubCkt" );  -- Default name
65        Port( CLOCK       : in    Std_Logic;
                CLR         : in    Std_Logic;
                ModeLatch   : in    Std_Logic;
                ProgValue   : in    Std_Logic_Vector(7 downto 0);
                pLOAD       : in    Std_Logic;
70              pSTEP       : in    Std_Logic;
                nTCOUT      : out   Std_Logic;
                pTCSS       : out   Std_Logic;
                nTCSS       : out   Std_Logic   );
        end component;
75
        end PECL_Comp;
```